AMENDMENT TO THE CLAIMS

Please add Claim 52 as follows:

1 to 21. (Cancelled)

22. (Original) A method for manufacturing a semiconductor device in which a plurality of electro-thermal conversion elements and a plurality of switching devices for flowing electric currents through said plural electro-thermal conversion elements are integrated on a first conductive type semiconductor substrate, said method comprising the steps of:

forming a second conductive type semiconductor layer on one principal surface of the first conductive type semiconductor substrate;

forming a gate insulator film on said semiconductor layer;

forming a gate electrode on said gate insulator film;

doping a first conductive type impurity by utilizing said gate electrode as a mask;

forming a semiconductor region by diffusing said first conductive type impurity; and

forming a second conductive type source region on the surface side of said semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region on the surface side of said second conductive type semiconductor layer.

23. (Original) A method for manufacturing a semiconductor device in which a plurality of electro-thermal conversion elements and a plurality of switching devices for flowing electric currents through said plural electro-thermal conversion elements are integrated on a first conductive type semiconductor substrate, said method comprising the steps of:

forming a second conductive type semiconductor layer on one principal surface of the first conductive type semiconductor substrate;

forming a field insulator film on said semiconductor layer selectively;

forming a gate insulator film on said semiconductor layer;

forming a gate electrode on said gate insulator film and said field insulator film;

doping a first conductive type impurity by utilizing said gate electrode as a mask;

forming a semiconductor region by diffusing said first conductive type impurity; and

forming a second conductive type source region on the surface side of said semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region on the surface side of said second conductive type semiconductor layer by utilizing said field insulator film as a mask.

24. (Original) A method according to claim 22 or 23, further comprising the steps of:

performing a first conductive type ion implantation into at least a channel region put between said source region and said semiconductor layer on the surface side of said semiconductor region through said gate electrode after said step of forming said semiconductor region; and

performing a heat treatment for activating the implanted impurity electrically.

25. (Original) A method according to claim 22 or 23, further comprising the steps of:

performing a first conductive type ion implantation into at least a channel region put between said source region and said semiconductor layer on the surface side of said semiconductor region through said gate electrode after said step of forming said semiconductor region; and

performing a heat treatment for activating the implanted impurity electrically,

wherein said ion implantation is ion implantation in which ions of boron are implanted in energy of 100 keV or more.

26. (Original) A method according to claim 22 or 23, wherein:

at least two of said drain regions of MIS type field effect transistors being switching devices are connected with one of said electro-thermal conversion elements, and

said sources of said plural MIS type field effect transistors are commonly connected.

27. (Original) A method for manufacturing a semiconductor device, said method comprising the steps of:

forming a second conductive type semiconductor layer on one principal surface of the first conductive type semiconductor substrate;

forming a gate insulator film on said semiconductor layer;

forming a gate electrode on said gate insulator film;

doping a first conductive type impurity by utilizing said gate electrode as a mask;

forming a semiconductor region by diffusing said first conductive type impurity; and

forming a second conductive type source region on the surface side of said semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region on the surface side of said second conductive type semiconductor layer,

wherein said method can obtain a transistor structure symmetrical to said source region.

28. (Original) A method according to claim 27, wherein said step of doping said first conductive type impurity includes a step of performing ion implantation obliquely to

said principal surface of said semiconductor substrate while rotating said semiconductor substrate.

29. (Original) A method according to claim 27, wherein said step of forming said second conductive type source region includes a step of performing ion implantation obliquely to said principal surface of said semiconductor substrate while rotating said semiconductor substrate.

30. (Original) A method according to claim 27, wherein said step of forming said second conductive type drain region includes a step of performing ion implantation obliquely to said principal surface of said semiconductor substrate while rotating said semiconductor substrate.

31. (Original) A method according to claim 27, wherein said step of doping said first conductive type impurity includes a step of performing ion implantation into said principal surface of an OFF substrate being said semiconductor substrate in a normal line direction of said principal surface.

32. (Original) A method according to claim 27, wherein said step of forming said second conductive type source region includes a step of performing ion implantation into said principal surface of an OFF substrate being said semiconductor substrate in a normal line direction of said principal surface.

33. (Original) A method according to claim 27, wherein said step of forming said second conductive type drain region includes a step of performing ion implantation into said principal surface of an OFF substrate being said semiconductor substrate in a normal line direction of said principal surface.

34. (Original) A method according to claim 27, wherein said step of doping said first conductive type impurity includes a step of performing ion implantation of boron in high energy of 100 keV or more.

35. (Original) A method for manufacturing a semiconductor device in which a plurality of insulated gate type field effect transistors are arranged in an array, said method comprising the steps of:

forming a second conductive type first semiconductor region on one principal surface of a first conductive type semiconductor substrate;

forming a gate insulator film on said first semiconductor region;

forming a plurality of gate electrodes on said gate insulator film;

forming a first conductive type second semiconductor region by diffusing a first conductive type impurity after implanting the impurity between adjoining two of said gate electrodes by using said two gate electrodes as masks at a fixed angle to a normal line direction of said semiconductor substrate while rotating said semiconductor substrate; and

forming a second conductive type source region in said second semiconductor region by utilizing said two gate electrodes as masks and a second conductive

type drain region severally in two of said first semiconductor regions disposed to put said second semiconductor region between them by implanting the impurity at the fixed angle to the normal line direction of said semiconductor substrate while rotating said semiconductor substrate.

36. (Original) A method for manufacturing a semiconductor device in which a plurality of insulated gate type field effect transistors are arranged in an array, said method comprising the steps of:

forming a second conductive type first semiconductor region on one principal surface of a first conductive type semiconductor substrate;

forming a field insulator film selectively on said first semiconductor region;

forming a gate insulator film on said first semiconductor region;

forming gate electrodes on said gate insulator film and said field insulator film;

forming a first conductive type second semiconductor region by diffusing a first conductive type impurity after implanting the impurity between two of said gate electrodes by using said two gate electrodes as masks at a fixed angle to a normal line direction of said semiconductor substrate while rotating said semiconductor substrate; and

forming a second conductive type source region in said second semiconductor region by utilizing said two gate electrodes as masks and a second conductive type drain region severally in two of said first semiconductor regions disposed to put said second semiconductor region between them by utilizing said field insulator film as a mask by

implanting the impurity at the fixed angle to the normal line direction of said semiconductor substrate while rotating said semiconductor substrate.

37. (Original) A method according to claim 35 or 36, wherein said second semiconductor region is formed deeper than said first semiconductor region.

38. (Original) A method according to claim 35 or 36, wherein a heating resistance element connected with said drain region electrically is formed.

39. (Original) A method for manufacturing a semiconductor device, said method comprising the steps of:

forming a second conductive type first semiconductor region on a first conductive type semiconductor substrate including one principal surface having a plane direction inclining against a lower dimensional plane direction;

forming a gate insulator film in said first semiconductor region;

forming a gate electrode on said gate insulator film;

forming a second semiconductor region by diffusing a first conductive type impurity after performing ion implantation of the impurity into said semiconductor substrate perpendicularly by utilizing said gate electrode as a mask; and

forming a second conductive type source region in said second semiconductor region by utilizing said gate electrode as a mask and a second conductive type

drain region in said second semiconductor region by performing ion implantation of impurities severally perpendicularly to said semiconductor substrate.

40. (Original) A method for manufacturing a semiconductor device, said method comprising the steps of:

forming a second conductive type first semiconductor layer on a first conductive type semiconductor substrate including one principal surface having a plane direction inclining against a lower dimensional plane direction;

forming a field insulator film in said first semiconductor region selectively;

forming a gate insulator film in said first semiconductor region;

forming a gate electrode on said gate insulator film and said field insulator film;

forming a second semiconductor region by diffusing a first conductive type impurity after performing ion implantation of the impurity into said semiconductor substrate perpendicularly by utilizing said gate electrode as a mask; and

forming a second conductive type source region in said second semiconductor region by utilizing said gate electrode as a mask and a second conductive type drain region in said second conductive type second semiconductor region by utilizing said field insulator film as a mask by performing ion implantation of impurities severally perpendicularly to said semiconductor substrate.

41. (Original) A method according to claim 39 or 40, wherein said plane direction of said principal surface of said semiconductor substrate inclines to said lower dimensional plane direction at a degree of a range from 3° to 10°.

42. (Original) A method according to claim 39 or 40, wherein said plane direction of said principal surface of said semiconductor substrate inclines to a (100) plane at a degree of a range from 3° to 10°.

43. (Original) A method according to claim 39 or 40, wherein said plane direction of said principal surface of said semiconductor substrate inclines to a (100) plane at an angle of 4°.

44. (Original) A method according to claim 39 or 40, wherein said step of forming said second semiconductor region diffuses said first conductive type impurity such that said impurity is deeper than said first semiconductor region.

45. (Original) A method according to claim 39 or 40, wherein a plurality of insulated gate type field effect transistor are arranged in an array.

46 to 51. (Cancelled)

52. (New) A method according to claim 22, wherein the drain region is formed separately from an end of the gate electrode.